Printable Die Attach Adhesives for Substrate-On-Chip Packaging

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ABSTRACT
The dominant trend in packaging DDR DRAM for the future is the face down substrate-on-chip configuration. For this type of package it is critical that the die attach method employed provide precise control of bond line thickness and die tilt, minimal fillet, and prevent contamination of the wire bond pads located on the edge of the center wire bond channel. To date, a film adhesive has been the die attach method of choice because it is well suited to meet those requirements. Unfortunately, films are quite expensive compared to die attach pastes in terms of material, process, and tooling costs. This is especially true when changes such as die shrinks and board redesigns mandate a taping tool change. To address this serious issue, a novel series of printable B-stage adhesives has been developed that deliver the performance of a film (with respect to bond line and flow control), with the low cost of a paste (in terms of tooling and materials).

In this paper, we will present data on a commercial series and a developmental series of printable adhesives, which were developed specifically for substrate-on-chip packages. These proprietary adhesives are formulated to be stencil printed on a substrate and then B-staged. The printed substrates then replace the standard pre-taped substrates that represent the mainstream in DRAM packaging. Data show that these printable adhesives deliver the performance of films, i.e. low flow and bond-line control on die attach, more than a six month storage life at room temperature, and do not require substrate pre-drying. ChipMOS Technologies has pioneered the assembly process using these adhesives and are seeing high UPH and equivalent reliability performance to film adhesives. Key in-package reliability data from those evaluations will be presented.

Key Words: die attach, stencil print, adhesive, packaging

INTRODUCTION
Typically the DDR DRAM packages in the substrate-on-chip (SOC) or board-on-chip (BOC) configuration utilize a plastic array type substrate bonded to the active face of the chip[1,2]. The substrate has a center slot cut out directly underneath the die through which wire bonding is performed to the opposite side of the substrate. A typical SOC package cross-section is shown in Figure 1.

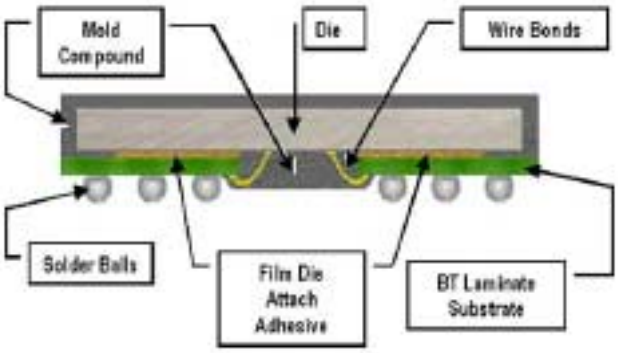

Figure 1. SOC Package Cross-Section

For this type of package it is critical that the die attach method employed provide precise control of bond line thickness and die tilt, minimal fillet, and prevent contamination of the wire bond pads located on the edge of the center wire bond channel. Typically two adhesive decals are used for die attach. They are rectangular in shape and are placed on either side of the center slot. On the outer perimeter, they may end just inside the die edge, at the die edge, or just beyond the die edge. In any case, it is critical that the adhesive be as close to the slot as possible to prevent a gap being left after molding. However, the wire-bond pads on the substrate are located right at the slot edge on the opposite side of the substrate. This requires both high accuracy in placing the adhesive, and very low controlled flow or filleting during die attach to prevent bond pad contamination. This combination of requirements necessitates a film type adhesive. Punching accuracy on pre-taping equipment is typically within 50 µm, and film adhesives can be made to flow less than 50 µm during attach, allowing the SOC package requirements to be met.

Along with the precise adhesive thickness and flow control a film adhesive provides, films can also offer advantages in UPH and work in process. Generally, film adhesives do not require substrate pre-drying, which eliminates a step from the process which is typically about four hours in length. Also, films are generally pre-attached to the substrate, which makes die bonding a high UPH process. Attach times for films are typically less than 1 sec. per die enabling die bonder UPH in the range of 500-2000.

Since the main stream packaging in DRAM over the last several years has been the TSOP II package (LOC configuration), the industry's infrastructure is also well

suited to the SOC package using film adhesives, as the process is quite similar and the equipment used can be the same.

Film die attach adhesives generally have the two drawbacks of cost and voiding. On the performance side, films tend to void either during attach or during cure, in no small part because they are usually unfilled. This means that compared to paste adhesives which are heavily filled with low moisture absorbing particles, the moisture absorption is significantly higher which can make the adhesive more prone to voiding. While current reliability requirements in the memory industry are usually only JEDEC Level 3, with 220-240ºC reflow (lower than for other packaging sectors), voids in the bond line can cause failures in reliability testing for almost any adhesive.

With respect to cost, film adhesive material cost tends to be several times higher than for a typical paste adhesive. Even more importantly, tooling costs for films are a significant part of the total package cost, especially when die shrinks, substrate redesigns, or R&D demands frequent tooling changes. Punching tools for taping adhesive to substrate can run several thousand dollars per machine, and typically a similar number of taping machines is required as there are die bonders, since UPH on the two processes are similar. This can mean that a cost of several hundred thousand dollars is incurred each time the tape decal is changed.

Nevertheless, to date film adhesives have been used almost exclusively for SOC packaging, as they have been the only readily available die attach adhesives suited to the package demands. However, the cost-driven nature of the memory packaging industry has created a demand for a lower total cost solution to SOC packaging. This paper presents data on a novel series of printable B-stage adhesives that deliver the performance of a film (with respect to bond line and flow control), with the low total cost of a paste (in terms of tooling and materials).

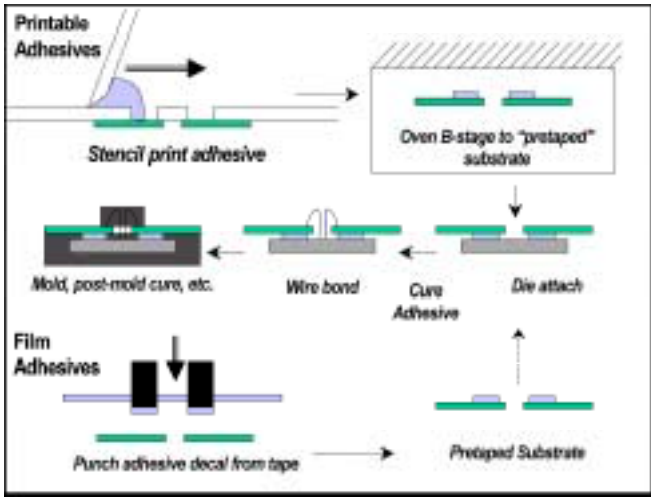

Figure 2. Process Flow Comparison for Printable and Film Die Attach Adhesives

3.0 Printable SOC Die Attach Adhesives

Printable die attach adhesives are used very similarly to film adhesives except in the application method initially employed to introduce the adhesive onto the substrate. The general process flow is shown in Figure 2. In the case of a printable adhesive, the material is stenciled onto the substrate. A subsequent oven B-stage process will reduce the adhesive thickness by removing the solvent leaving only solid adhesive resins behind. At this point, there is no difference in either physical make up or performance between this material and a film adhesive.

3.1 Material Selection

Several adhesives are discussed in this paper. Each material has been designed with particular process considerations in mind. The main processing factors that will determine the appropriate material selection are:

- the type of die bonder available (LOC, flip chip or other),
- the stencil printing site (printing at the assembly house or at the substrate manufacturer),
- whether the die bonding process is magazine-to-magazine or stack-to-magazine, and
- the amount of flow allowable or desired during die attach.

Specifically, four adhesives will be discussed. Their properties while in paste form are shown in Table 1.

Paste Properties				
	Com A	***Dev A***	***Dev B***	***Dev C***
Filler Type	Silica	Silica	Silica	Silica + TiO_2
Chemistry	Epoxy + proprietary chemistry	Epoxy + proprietary chemistry	Epoxy + proprietary chemistry	Epoxy + proprietary chemistry
Solvent	Carbitol Acetate (CA)	CA	CA	CA + cyclohepta none
Viscosity (25ºC / 5 rpm)	27,00 cP	32,000 cP	43,000 cP	53,000 cP
Thixotropic Index	2.7	4.6	5.0	4.1
Estimated Work Life (25ºC)	7 days	2 days	2 days	2 days
Open Time (<25% viscosity increase)	16 hours	16 hours	16 hours	8 hours
Estimated Storage Life	6 mos @ -40ºC	6 mos @ -40ºC	6 mos @ -40ºC	6 mos @ -40ºC
Recom-mended B-stage Conditions	60 min @ 120ºC	60 min @ 120ºC	60 min @ 125ºC	30 min @ 100ºC

Table 1. Printable Adhesive Properties

3.1.1 LOC Die Bonders

Since main stream DRAM manufacture uses LOC Tape for the TSOP II package, most assembly facilities for DRAM are equipped with LOC die bonders. The SOC package configuration is quite similar to the LOC package, so these die bonders are well suited to SOC packaging. LOC die bonders typically require > 20N (2 kg_f) per die in order to be well within the control range of the equipment. At the same time, the SOC package geometry typically restricts flow during attach, or filleting, to <50 µm in width. Therefore, the adhesive selected for such a process must be attached at a force of more than 20N (2 kg_f) without flowing more than 50 µm during the process. Also, the substrates on most LOC die bonders are fed in as a stack, with one substrate directly contacting the adhesive from the next one. This requires an adhesive that is tack-free. Dev B and Dev C meet the requirements for this type of process. The tack-free nature of these adhesives may also allow printing to be performed at the substrate manufacturer replacing pre-taping so assembly houses can receive substrates with pre-applied adhesive as is typical for LOC assembly.

3.1.2 Other Film Die Bonders:

Some SOC assembly is being performed on other types of die bonders compatible with film, such as flip chip die bonders. These bonders can typically deliver only an intermediate amount of force (10-20 N or 1-2 kg_f /die), and are usually fed by magazines containing the substrates. Since the substrates do not contact each other, some tackiness to the adhesive may be allowed for this type of process, and the lower force capability necessitates a slightly higher flow material with better wetting characteristics. Dev A has been designed for such a process.

In still other processes, standard paste die bonders are converted for film by adding a heating block. These bonders can typically only deliver < 1 kg_f /die during attach, and Com A adhesive works well in such a process.

3.2 Material Storage and Handling:

Due to the high volumes involved in DRAM manufacture, ease of material handling is extremely important. Long shelf lives, work lives and open times are critical. Our commercial series and the developmental series adhesives are shipped as a solvent-based paste. They need to be stored frozen (-40ºC), just as standard die attach pastes. However, once defrosted, they have very long work lives. As seen in Table 1, the room temperature work life ranges from 2 days to a week for these materials. The open time is defined as the time during which <25% viscosity change is seen once the material has been exposed to the atmosphere at room temperature, or once it has been removed from its original packaging. This property relates very closely to the print life, though the print life also depends heavily on the manufacturing environment and printing parameters. Open times for these materials are very long (more than one shift), which enables high volume printing to be implemented with minimized material waste and cleaning time.

3.3 Printing and B-staging:

The commercial series and the developmental series adhesives exhibit outstanding printing characteristics. These materials allow very high definition printing with minimal bleed or spreading on a variety of substrates, most especially BT laminate boards (which are used in most SOC packaging) with or without solder mask coatings in the bond area. The adhesives contain about 70% solids. During B-staging, the solvent is dried out, reducing the overall thickness by 35-40%. The overall bond-line thickness may therefore be controlled by the stencil thickness. Figure 3 shows a non-contact laser profilometer scan for Dev A after printing through a 50 µm thick stencil and B-staging. As seen, the adhesive pads are extremely flat, with no visible tailing, sharp walls and an average thickness of around 33 µm, representing a reduction of thickness of around 34%. ChipMOS Technologies uses a 75 µm stencil to print Com A adhesive resulting in a thickness of 45-50 µm after B-stage and a final bond-line thickness of around 40-45 µm. This is the recommended thickness for optimum reliability performance for most SOC type packages.

Figure 3. Laser Profilometer Scan of Dev A After B-staging

Printing of the commercial series and the developmental series adhesives should be performed using a stainless steel squeegee with an angle of 45-60 degrees and a speed of 2-6 in./sec. After printing, the substrates should be B-staged as soon as possible, though ChipMOS has studied the dwell time (time between printing and B-staging) for Com A adhesive and its effect on subsequent processing and found no adverse effects for times higher than 48 hrs. This is important, as oven availability or lot size may dictate that the substrates will see extended dwell times, and that the times may vary significantly throughout a batch.

Although the solvent is generally the same throughout the adhesive series, recommended B-stage times do vary from material to material. The unique chemistry of this adhesive series (US Patent pending[3]) which provides minimal voiding and high reliability requires different B-stage times depending on the material. All recommended B-stage

conditions are significantly below the cure onset for the materials.

Once B-staged, the printed adhesive may be stored at room temperature for an estimated 6 months, which is generally the requirement for substrates with pre-applied adhesive in the memory packaging industry. Data for storage of Dev B through 5 months at room temperature after B-stage is shown below in Table 2. This study is ongoing and data are still being accumulated.

Storage Time @ Room Temperature	Flow During Die Attach (%) ***	Wet – Out (%) **	Green Strength* (kg/cm^2)
Initial	1	100	119
1 day	1	100	113
1 week	0	95	109
2 weeks	0	95	106
3 weeks	0	100	110
1 mo	0	100	113
2 mos	3	100	134
3.5 mos	3	95	119
mos	0	90	140

Table 2. Room Temperature Storage Life of Dev B After B-staging

** Green strength (GS) is defined as the die shear strength before cure and is measured on a 2x2 mm die.*
*** % wet-out is measured using a 7x7 mm glass die for die attach and then viewing the die under a microscope at 10x magnification*
**** % flowduring attach is measured by printing a 12.7 mm wide adhesive on a glass slide, performing die attach with 3 dies (7x7mm), and then measuring the average amount of widening of the adhesive line under the dies.*
NOTE: Die attach was performed on a 7x7mm die at 150ºC, 2.5 kg_f, 1 sec. Attach, Criteria for acceptable performance are <5% flow, >90% wet-out, >100 kg/cm^2 GS

Optimum attach conditions and properties of the adhesives after B-stage are shown in Table 3.

Properties After B-Stage				
	Com A	Dev A	Dev B	Dev C
Weight Loss @ 200º(TGA)	0.67%	0.50%	0.48%	1.10%
Recommen-ded Cure Condition	30 min ramp to 175ºC, 60 min @ 175ºC	30 min ramp to 175ºC, 60 min @ 175ºC	30 min ramp to 175ºC, 60 min @ 175ºC	30 min ramp to 175ºC, 60 min @ 175ºC
Recommen-ded Attach Temperature	110ºC – 130ºC	130ºC – 160ºC	150ºC – 180ºC	150ºC - 200ºC
Recommen-ded Attach Force (7x10 mm die)	0.5 – 1.0 kg	0.5 – 1.5 kg	3 – 5 kg	2 – 6 kg
Recommended Attach Time	< 1 sec.	< 1 sec.	< 1 sec.	75 – 500 msec.
Estimated Storage Life (25ºC)	6 months	6 months	6 months	6 months

Table 3. Printable Adhesive Attach Conditions and Properties After B-Stage

3.4 Die Attach and Cure

Due to the unique chemistry of these adhesives, they demonstrate excellent performance at die attach. Minimal voiding is seen with good wet-out, controlled flow and broad process windows. Figures 4 and 5, respectively, show the die attach process windows for Dev A and Dev B. For this experiment, 7x7 mm Si dies were used on a BT substrate with solder mask, and the chip attach delay time was held constant at 1 sec. The criteria for a set of conditions to fall within the recommended process window is <5% voiding and flow and >90% wet-out. The figures show that both materials have very broad process windows for die attach with Dev B generally requiring higher process temperatures and pressures than Dev A.

Dev C was designed specifically for high UPH die attach processing. Due to the lower fumed silica filler content, shorter B-stage time, and the nature of the resin system, it can be attached with chip attach delay times significantly lower than 1 sec. (50-400 msec.). This product is recommended for processes with a bottleneck at die attach, but should not be used on large dies (>7x12 mm) due to its higher modulus.

All of these adhesives should be cured for 1 hr. @ 175ºC to achieve full curing. A 30 minute ramp up time is recommended in order to ensure minimal voiding, though these materials are not prone to increased voiding during die attach cure. Some or all of this cure time may coincide with

the post-mold curing, depending on process demands after die attach. Also, lower curing temperatures may work, again depending on process demands on the die attach material. The cure schedule needs to be optimized on an individual basis depending on process, package geometry and warpage considerations.

Die Size 7 x 7 mm – 1 sec. attach time used in all cases							
Temp vs. Force		0.50 kg	0.75 kg	1.0 kg	1.5 kg	2.0 kg	2.5 kg
120ºC	% Voids	0%	0%	0%	0%		
	% Flow	0%	0%	< 1%	< 3%		
	%Wet-out	80%	85%	90%	95%		
130ºC	% Voids			0%	0%	0%	0%
	% Flow			< 1%	< 3%	< 5%	8%
	% Wet-out			95%	100%	100%	100%
140ºC	% Voids			0%	0%	0%	
	% Flow			< 1%	< 3%	8%	
	% Wet-out			95%	100%	100%	
150ºC	% Voids	0%	0%	0%	0%	0%	
	% Flow	< 1%	< 1%	< 3%	5%	10%	
	% Wet-out	80-90%	95%	100%	100%	100%	
160ºC	% Voids	0%	< 1%	< 1%	< 1%		
	% Flow	< 1%	< 3%	5%	15%		
	% Wet-out	90%	100%	100%	100%		
170ºC	% Voids	0%	0%	< 1%	< 1%		
	% Flow	< 1%	< 1%	5%	15%		
	% Wet-out	90%	95%	100%	100%		

Poor wet-out
Recommended Process Window
Excessive Flow or Voiding

Figure 4. Die Attach Process Window for Dev A

Properties of the adhesives in their final cured state are shown in Table 4. All these materials have high adhesion strength, especially at elevated temperatures that simulate solder reflow conditions. They also have low ionic impurity levels, which is critical since they are being attached to the active surface of the Si die. The low glass transition temperature of these adhesives makes them tough, compliant materials throughout the range of use and processing temperatures. Their coefficients of thermal expansion are somewhat lower than for typical epoxy adhesives, resulting in relatively low package stress. Also, the moisture resistance is very good. Com A, for example, retains 75% of its room temperature adhesion strength after 48 hr. exposure to 85ºC, 85% RH, and 65% of its adhesion strength at 245ºC. All these properties contribute to the outstanding reliability performance exhibited by this series of adhesives.

Die Size 7 x 7 mm – 1 sec. attach time used in all cases						
Temp vs. Force		1.5 kg	2.0 kg	2.5 kg	3.0 kg	3.5 kg
140ºC	% Voids		0%			0%
	% Flow		0%			< 3%
	% Wet-out		50%			90%
150ºC	% Voids		0%		0%	0%
	% Flow		0%		0%	< 3%
	% Wet-out		50%	75%	90%	100%
160ºC	% Voids		0%	0%	0%	0%
	% Flow		0%	0%	< 2%	< 5%
	% Wet-out		60%	90%	95%	100%
170ºC	% Voids		0%	0%	0%	< 3%
	% Flow		0%	< 2%	< 5%	< 10%
	% Wet-out		80%	90%	95%	100%
180ºC	% Voids	0%	0%	0%	0%	0%
	% Flow	0%	0%	< 3%	< 5%	< 10%
	% Wet-out	90%	95%	100%	100%	100%

Poor wet-out
Recommended Process Window
Excessive Flow or Voiding

Figure 5. Die Attach Process Window for Dev B

3.5 Package Reliability:

These printable adhesives have shown excellent reliability performance to date. The current MRT standard for most memory devices is JEDEC Level 3 with a reflow temperature of either 220ºC or 240ºC. However, most new packages are being qualified at Level 3, 260ºC reflow in order to meet Pb-free packaging requirements. Com A series and the developmental series adhesives have been shown not only to meet, but exceed this standard. ChipMOS Technologies has qualified Com A on several DRAM devices at JEDEC Level 3/220ºC. Additionally, they have tested package reliability at Level 3/260ºC and at Level 2/220ºC on their SOC 60B 256Mb SDRAM package and both tests passed. Higher reliability has not been tested at ChipMOS. Results of the Level 3, 260 test are shown in Figure 6. Elsewhere, Dev A has passed JEDEC Level 2/260ºC reflow, and Dev B has passed JEDEC Level 3/245ºC reflow on similar packages. Again, no higher reliability levels were tested.

Properties After Cure					
		Com A	Dev A	Dev B	Dev C
Ionics (ppm)	Na	4	4	2	1
	K	N/D*	N/D*	N/D*	N/D*
	Cl	13	12	9	5
Dynamic Tensile Modulus (MPa)	25ºC	950	1100	1600	2100
	150ºC	20	53	130	160
	250ºC	9.7	15	24	21
Die Shear Strength 2x2 mm die (kg/cm²)	25ºC	463	535	453	575
	245ºC	73	78	63	100
Tg	TMA	-10ºC	-16ºC	67ºC	17ºC
CTE (ppm/ºC)	Below Tg	94	72	83	58
	Above Tg	237	187	205	139

Table 4. Typical Stencil Print Adhesive Properties After Cure

- *N/D = value is below the detectable limit (~1ppm)*

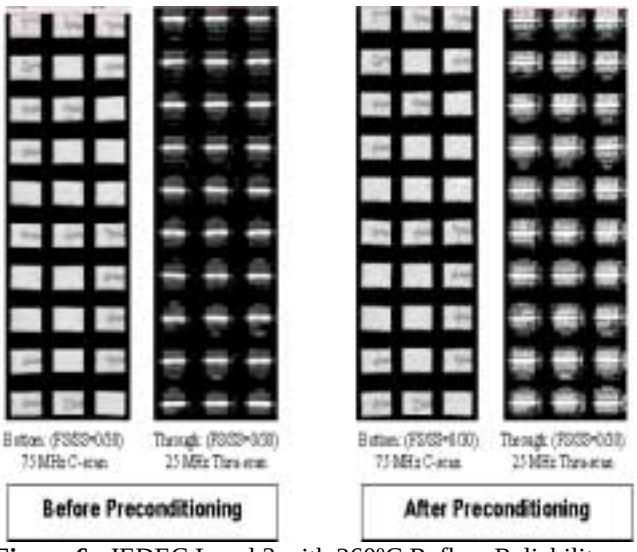

Figure 6. JEDEC Level 3 with 260ºC Reflow Reliability Results for ChipMOS' SOC 60B 256Mb SDRAM Package

No delamination is observed after preconditioning and solder reflow

ChipMOS Technologies' SOC 60B 128Mb and 256Mb SDRAM packages have also passed the following reliability tests:

1000 hours High Temperature Storage	HTS	150ºC
1000 hours Temperature, Humidity, Bias	THB	85ºC / 85% RH / 3.6V
240 hours Pressure Cooker Test	PCT	121ºC / 100% RH / 2 atm
1000 cycle Thermal Cycle Test	TCT	-65ºC to + 150ºC in air
100 hours Highly Accelerated Stress Test	HAST	130ºC / 85 RH / 3.6V

4.0 Conclusions

New novel printable adhesives have been developed to replace traditional film adhesives for low cost SOC-type memory packaging. These commercial series and developmental series adhesives are printed onto the substrate and then oven B-staged to provide substrates with pre-applied adhesive for DRAM packaging. The adhesives provide at least equivalent performance to commercially available films at every process step and in package reliability. Significant savings can be realized by using such adhesives through lower material costs and lower process and tooling costs. The adhesives have been designed to fit the existing packaging infrastructure for main stream DRAM device manufacture. Com A is now qualified at ChipMOS on various SDRAM and DDR DRAM devices and is in mass production.

5.0 References

1) US Patent # 6048755; Issued to Micron in 2000
2) TW Patent # 447094; Issued to ChipMOS in 2001
3) US Patent Application # 10/016,844; Submitted by Ablestik